News Release

Memory IP Characterization for 45nm Technology and below

Address power-gating, data retention, pin power, multiple voltage supplies, ECSM/CCSM models, efficient layout extraction and circuit simulation.

SANTA CLARA, Calif., May 21, 2007 – Legend Design Technology, Inc. today announced that its CharFlo-Memory!, an automatic memory characterization tool suite, has been upgraded with new capabilities for the designs of 45nm and below. The new release addresses the power gating, data retention, pin power, multiple voltage supplies, ECSM/CCSM models, efficient layout extraction and circuit simulation. The CharFlo-Memory! tool suite consisting of SpiceCut, MemChar and MSL Manager provides the benefits of accuracy, throughput and automation.

"For 45nm memory compilers at Freescale, we have successfully built Legend Design's SpiceCut™ into our memory characterization flow, which is based on layout reality. Without Legend Design's tools, we would not have achieved these aggressive production goals." said Gary Hancock, Sr. CAD/Flow Engineer, Freescale Semiconductor, Inc.

For 45nm technology and below, memory IP characterization need face the following challenges

1. New low-power and low-leakage designs (e.g. power-gating and data retention)
2. Sophisticated memory modeling (e.g. pin power and ECSM/CCSM)
3. Large layout-extracted circuit with resistors and capacitors, and
4. Long circuit simulation time due to complex Spice models (e.g. well-proximity and stress effects)

With extensive R&D efforts and field experiences, we have successfully developed the solutions for the above challenges and built the codes into CharFlo-Memory! tool suite for characterizing 45nm memory IP. The following are the detailed descriptions.

1. Power-gating characterization
   Power-gating is a technique for reducing leakage power by controlling the supply voltage to active portions of the design. When characterizing the power-gating parameters such as ramp-up and ramp-down time, the detailed circuit simulation on the complete circuit including all related memory cells and their capacitive effects shall be required. The SpiceCut can accurately produce small critical-path circuits with multipliers on repeated cells for characterizing power-gating completely.

2. Data Retention analysis
   Data retention voltage is the standby supply voltage minimized for retaining the data stored in memory cells. Since retention voltage is quite lower than the voltage supply, leakage current will be substantially reduced in memory circuits. To achieve the safe level of reliability, the stability analysis on retention voltage and related control circuits must be performed with detailed circuit simulations. The SpiceCut can

automatically produce small and accurate critical-path circuits, which enables fast and precise simulation for the data retention analysis.

3. Pin power characterization

   The power dissipation of on-chip memory IP is generally calculated by the sum of ‘pin power’ on those pins having logic transitions. For each pin, SpiceCut can automatically produce a small and accurate critical-path circuit for ‘pin power’ characterization. The critical-path circuits for clock pin will include all related clock tree and mesh circuits.

4. ECSM and CCSM support
   By taking the output driver as a current source rather than a voltage source, ECSM/CCSM can provide accurate timing modeling for 45nm technology. CharFlo-Memory! will provide both ECSM and CCSM models, in addition to the ‘.Lib’ model.

5. Critical-net layout extraction
   For large memory IP, layout parasitic extraction can take an excessive amount of time and generate huge amounts of circuit data. By providing 'critical nets' to extract, CharFlo-Memory! enables layout parasitic extraction on critical-path circuits only. Since the 'critical nets' are less than 1% of the total nets on chip, the time-consuming layout parasitic extraction can be done in a much shorter time, with a significant decrease in the amount of extracted circuit data.

6. Critical-path circuit building
   With the 45nm technology and below, the device model becomes more complex and simulation time gets much longer. Through building critical-path circuits, the detailed simulation on complex models can then be executed efficiently. The SpiceCut can automatically produce small and accurate critical-path circuits for characterizing access time, setup and hold time, minimum clock cycle time, input pin capacitance, output pin loading, dynamic power etc.

CharFlo-Memory! tool with new capabilities for the designs of 45nm and below will be available in Q3, 2007.

About Legend

Legend Design Technology Inc. is a leading provider of circuit simulation and semiconductor IP characterization software for SoC designs. With an emphasis on productivity and value, Legend’s CharFlo-Memory! toolset revolutionizes the time-consuming and error-prone processes associated with characterization. MSIM is Legend’s high-accuracy SPICE circuit simulator with great convergence and extensive model support. Turbo-MSIM is Legend’s full-chip FastSpice circuit simulator ideal for timing and power simulation, and function verification. Both simulators are well designed for nanometer technology challenges, and provide excellent price performance. For more information, visit www.LegendDesign.com.

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CONTACTS:
Legend Design Technology Inc.
Jane Wei
Manager
408-748-8888 X234
JaneW@LegendDesign.com